

Instruction scheduling for VM client compilers

In a recent project an object oriented layer between low-level intermediate representation and binary code has been developed for the Maxine compiler, that allows easy reordering and dependency tracking of instructions before they are written. This task consists of implementing an instruction scheduler on top of this data structure.

Exact extent of this work will be determined with the supervisor. It is most suitable for master thesis work.

Goals

- measurable improvements on the peak performance for at least one benchmark for either SpecJVM98 or DaCapo2006 (or any other benchmark in coordination with the advisor)

Tasks

- literature study on instruction scheduling, heuristics
- CPU architecture study to prototype a framework
- model at least one CPU architecture in your scheduler

Other information

- on Hotspot: programming language: Java (with C1X/Graal), alternatively C++ (with Hotspot C1)
- best results can be obtained on an (mostly) in-order architecture, e.g. an Atom CPU

Further information

Thomas Schatzl, HF305, thomas.schatzl@jku.at